PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Seigo NISHIKAWA, et al.

Appln. No.: 10/781,911

Confirmation No.: 5337

Filed: February 20, 2004

For: ARC WELDER

Docket No: Q79997

Group Art Unit: 1725

Examiner: Clifford C. Shaw

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of $500.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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23373
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Date: September 28, 2006

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Sir:

In accordance with the provisions of 37 C.F.R. § 41.37 Appellants are submitting an Appeal Brief to appeal from the Final Office Action dated February 1, 2006 (hereinafter "the -Final Office Action"), wherein rejection of claims 1-3 have been maintained. This Appeal Brief is accompanied by a Submission which includes the required appeal fee set forth in 37 C.F.R. § 41.20(b)(2). Appellants' Notice of Appeal was filed on July 28, 2006.

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I. REAL PARTY IN INTEREST

The real parties in interest are KABUSHIKI KAISHA YASKAWA DENKI and HITACHI VIA MECHANICS, LTD. (Assignees) by virtue of an assignment executed by Seigo NISHIKAWA, Seiichiro FUKUSHIMA, Tsuneo SHINADA and Kiyoshi NAITO, the co-inventors on February 16, 2004, and recorded by the Assignment Branch of the U.S. Patent and Trademark Office on February 20, 2004 (at Reel 015010, Frame 0706).

II. RELATED APPEALS AND INTERFERENCES

Upon information and belief, there are no other prior or pending appeals, interferences, or judicial proceedings known to Appellants, Appellants' representatives or the Assignee that may be related to, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Each of pending claims 1-3 are finally rejected (see Final Office Action dated February 1, 2006).

IV. STATUS OF AMENDMENTS

There are no pending unentered amendments in this case.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to an arc welder that conducts both short circuiting arc welding and pulsed arc welding. The claimed subject matter is exemplified in Fig. 2 of the specification. A first rectifier circuit 2 converts an alternating current 1 to a direct current. An inverter circuit 3 then converts the direct current to a high-frequency alternating current. Next a transformer 4 converts the output from the inverter circuit 3 to a voltage suitable for arc welding. (*See* Specification p. 6, lines 15-21.)

A current circuit 10 is connected in parallel to a second rectifier circuit 5 (*See* Specification p. 7, lines 3-4). The transformer 4 applies a higher voltage to the current circuit 10 compared to the rectifier circuit 5. This is achieved by providing a secondary winding with more turns for the current circuit 10, and a secondary winding with fewer turns for the rectifier circuit 5. For example, Fig. 2 shows that the secondary winding for the current circuit 10 contains 3 turns, whereas the secondary winding for the rectifier circuit 5 contains only 2 turns. In addition, an output voltage of the current circuit 10 is higher than an output voltage of the second rectifier circuit 5. (*See* Specification p. 9, lines 19-24.)

The second rectifier 5 converts the voltage from the transformer 4 to a direct current, which passes through a first DC reactor 6 (*See* Specification p. 6, lines 20-23). Within the current circuit 10, a third rectifier circuit 12 converts the voltage from the transformer 4 to a direct current, which passes through a second DC reactor 13, and then through the first DC reactor 6. The direct current is then supplied to the arc welding portion. The current circuit 10

also comprises a current controlling circuit 11, which contains semiconductor elements with ON/OFF gates. (*See* Specification p. 7, lines 5-15.)

The current circuit 10 has a higher reactance than the first reactor 6. For example, the second DC reactor 13 within the current circuit 10 may have a large reactance of 100-2,000 μH (*See* Specification p. 7, lines 15-16). In contrast, the first reactor 6 may have a small reactance of 20 μH or less (*See* Specification p. 7, lines 1-2). By supplying a current when the welding current is reduced, the second DC reactor 13 prevents arc interruption during welding (*See* Specification p. 8, lines 11-14). A controlling circuit 17 regulates the current that flows to the third rectifier circuit 12 and the second DC reactor 13 (*See* Specification p. 8, lines 19-23).

As discussed above, a higher voltage is applied to the current circuit 10 than the rectifier circuit 5. This allows a larger amount of current to be supplied to the third rectifier circuit 12 and the second DC reactor 13, which prevents arc interruption from occurring during the short circuiting arc welding operation. Therefore, both short circuiting arc welding and pulsed arc welding can be performed by a single welder. (*See* Specification p. 9, line 27 - p. 10, line 23.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The only issue on appeal is whether the rejection of claims 1-3 under 35 U.S.C. 103(a) based on Terayama et al. (U.S. Patent No. 5,645,741; hereinafter "Terayama"), in view of Stava (U.S. Patent No. 5,148,001), is proper.

VII. ARGUMENT

A. Independent Claim 1 is Unobvious in View of the combined teachings of Terayama and Stava

Appellants submit that the Examiner improperly finally rejected Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Terayama in view of Stava. Appellants respectfully request the Board to reverse this final rejection at least because of the following arguments.

Claim 1 recites an arc welder with a rectifier circuit that converts an alternating current to a direct current. An inverter circuit converts the output of the rectifier circuit to a high-frequency alternating current. A transformer converts the output of the inverter circuit to a voltage suitable for arc welding. A second rectifier circuit rectifies the output of the transformer to a direct current. A first reactor is connected to the second rectifier circuit.

Importantly, a current circuit is connected in parallel to the second rectifier circuit, and has a reactance that is larger than a reactance of the first reactor. In addition, a voltage that is applied to the current circuit from the transformer is higher than a voltage that is applied to the second rectifier circuit from the transformer. Also, an output voltage of the current circuit is higher than an output voltage of the second rectifier circuit.

In rejecting claims 1-3 of the present invention, the Examiner argues:

> In regard to the claim language specifying that the voltage applied to the current circuit is higher than the voltage applied to the second rectifier circuit and specifying that the output voltage of the second rectifier circuit is higher than the current circuit output, the same does not patentably distinguish over Terayama et al. (5,645,741). Figure 2 in Terayama et al. (5,645,741) clearly shows that the open circuit output voltage of the auxiliary power source (i.e., the power source associated with element DR4) is higher than the open circuit voltage of the main power source (i.e., the source

> associated with DR2). The only way for this to happen is if the secondary voltage from T1 into DR4 is higher than the voltage into DR2, satisfying the claim language.

Final Office Action at page 3.

The Examiner further contends:

> Applicant argues that his claims distinguish over Terayama et al. (5,645,741) because of the language directed to the different voltages applied to the current circuit and to the second rectifier circuit. This argument is not persuasive. In the voltage/current graphs in Fig. 3 of Terayama et al. (5,645,741) clearly shows that his auxiliary power supply has a larger open circuit voltage than the main power supply. Since both the auxiliary and main power supplies are connected to the same transformer primary, the only way to achieve this difference in voltages is by providing different secondary windings for T1, with a higher voltage being provided to the auxiliary source to achieve the disclosed higher output voltage.

Final Office Action at page 4. The Appellants respectfully disagree with the Examiner's arguments.

Contrary to the Examiner's assumptions, Fig. 3 of Terayama clearly shows that the inverter transformer T1 has the *same* number of turns in the secondary windings providing power to the auxiliary rectifier DR4 and the secondary rectifier DR2. Therefore, transformer T1 applies the *same* voltage to the auxiliary rectifier DR4 and the secondary rectifier DR2. This is required by Faraday's Law, which says that in a transformer:

$$\frac{V_s}{V_p} = \frac{N_s}{N_p}, \qquad (1)$$

where V_s is the secondary voltage, V_p is the primary voltage, N_s is the number of turns in the secondary winding, and N_p is the number of turns in the primary winding. Because Terayama uses the same transformer T1 to supply power to both the auxiliary rectifier DR4 and the

secondary rectifier DR2, the primary voltage V_p and number of turns N_p are the same for both circuits. Also, as Fig. 3 shows, the secondary winding for the auxiliary rectifier DR4 has the same number of turns N_s as the secondary winding for the secondary rectifier DR2. Therefore, according to Eq. (1), the same voltage is applied to both the auxiliary rectifier DR4 and the secondary rectifier DR2.

Further, the specification of Terayama does not discuss the number of turns in each secondary winding of transformer T1. The Examiner's contention that different secondary windings are provided in transformer T1 for the auxiliary rectifier DR4 and the secondary rectifier DR2 is incorrect. It is common practice to represent a different number of turns in a winding with a different number of loops in a schematic diagram. For example, in an earlier portion of the final rejection, the Examiner argues that the inductance of the reactor LD2 is larger than the inductance of the reactor LD1, because the circuit diagram in Fig. 3 of Terayama shows that the reactor LD2 has a greater number of turns than the reactor LD1 (*See* Final Office Action at page 2). Terayama's use of a schematic representation with a different number of loops for the reactors suggests that if the secondary windings of the transformer T1 had different numbers of turns, Fig. 3 would reflect this with a different number of loops in a schematic representation of the secondary windings. Instead, Fig. 3 clearly shows that there is a 1:1 ratio of turns between the secondary winding for the auxiliary rectifier DR4 and the secondary rectifier DR2.

In contrast, Figs. 1 and 2 of the present Specification clearly show that the secondary winding for the current circuit 10 has ***more*** turns than the secondary winding for the second rectifier circuit 5. In fact, Figs. 1 and 2 illustrate that there is a 3:2 ratio of turns between the secondary winding for the current circuit 10 and the secondary winding for the second rectifier circuit 5. This embodies the requirement of claim 1 that a voltage applied to the current circuit is

higher than a voltage applied to the second rectifier circuit. The purpose of applying a higher voltage to the current circuit than the second rectifier circuit is to prevent arc interruption during short circuiting arc welding operation (*See* specification p. 9, line 19 - p. 10, line 23).

In addition, Terayama does not teach or suggest that the output voltage of the auxiliary rectifier DR4 is always *higher* than the output voltage of the secondary rectifier DR2, as required by claim 1. Instead, Fig. 2 of Terayama shows that the output voltage of the auxiliary power source, which contains the auxiliary rectifier DR4, is *lower* than the output voltage of the main power source, which contains the secondary rectifier DR2, when the current is set to Is3, as well as for some lower values of the current.

In summary, Terayama does not teach or suggest that the transformer T1 applies a higher voltage to the auxiliary rectifier DR4 than the secondary rectifier DR2, as required by claim 1. In addition, Terayama does not teach or suggest that the output voltage of the auxiliary rectifier DR4 is always higher than the output voltage of the secondary rectifier DR2, as further required by claim 1.

Likewise, Stava fails to overcome the deficiencies noted in the teachings of Terayama.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner has not satisfied the burden of establishing *prima facie* obviousness at least because he has not satisfied the "all limitations" prong of the three prong test for obviousness. Specifically, the Examiner has not shown that the combined teachings of Terayama and Stava suggest the invention as a whole including at least the limitations that are discussed above.

Since the "all limitations" test is not satisfied, the "motivation" and the "reasonable expectation of success" prongs of the test for obviousness must also fail.

Therefore, the Examiner's finding of obviousness of claim 1 based on the combined teachings of Terayama and Stava must be reversed.

Claims 2 and 3 are patentable over Terayama and Stava at least by virtue of their dependency on claim 1. Therefore, their rejection must also be reversed.

VIII. CONCLUSORY REMARKS

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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CLAIMS APPENDIX

CLAIMS 1-3 ON APPEAL:

1. An arc welder having: a rectifier circuit which rectifies an alternating current to a direct current; an inverter circuit which converts an output of said rectifier circuit to a high-frequency alternating current; a transformer which converts an output of said inverter circuit to a voltage suitable for arc welding; a second rectifier circuit which rectifies an output of said transformer to a direct current; and a first reactor which is connected to said second rectifier circuit, wherein

said arc welder comprises a current circuit which is connected in parallel to said second rectifier circuit with a reactance that is larger than a reactance of said first reactor,

wherein a voltage that is applied to the current circuit from the transformer is higher than a voltage that is applied to the second rectifier circuit from the transformer, and

an output voltage of the current circuit is higher than an output voltage of the second rectifier circuit.

2. The arc welder according to claim 1, wherein said reactance of said first reactor is 20 μH (microhenries) or smaller, and said reactance of said current circuit which is connected in parallel to said second rectifier circuit is 100 μH or larger.

3. The arc welder according to claim 1 or 2, wherein said current circuit which is connected in parallel to said second rectifier circuit comprises:

a current controlling circuit which controls a current;

a third rectifier circuit which rectifies said controlled current; and

a second DC reactor which is connected to said third rectifier circuit.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.